Transmit / Receive Modules

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Unclassified

Report Documentation Page

Form Approved
OMB No. 0704-0188

1. REPORT DATE	2. REPORT TYPE	3. DATES COVERED
01 MAY 2007	**N/A**	**-**

4. TITLE AND SUBTITLE
UnclassifiedTransmit / Receive ModulesTransmit Modules

5a. CONTRACT NUMBER

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)

5d. PROJECT NUMBER

5e. TASK NUMBER

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
PEO IWS 2.0 Above Water Sensors Directorate Naval Sea Systems Command

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

10. SPONSOR/MONITOR'S ACRONYM(S)

11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release, distribution unlimited

13. SUPPLEMENTARY NOTES
See also ADM202171., The original document contains color images.

14. ABSTRACT

15. SUBJECT TERMS

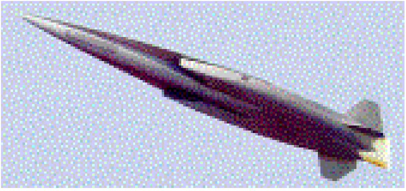
16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			
unclassified	**unclassified**	**unclassified**	**UU**	**15**	

Standard Form 298 (Rev. 8-98)
Prescribed by ANSI Std Z39-18

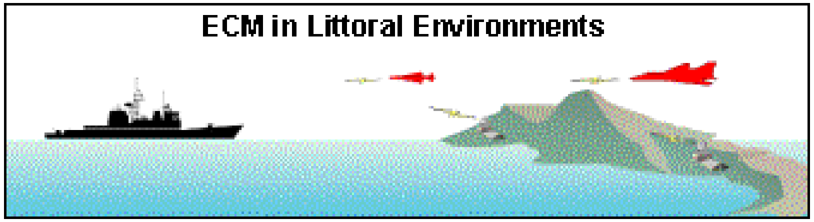
T/R Module Outline

- Future surface navy radar
- Performance and cost
- Wide bandgap semiconductors
- Summary

Radar System Performance Drivers



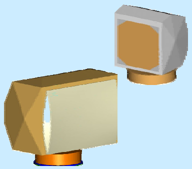
- **Littoral Operations**
- **AAW Threats**
  - Stealth
  - Speed
  - Altitude
  - Maneuvers
  - Countermeasures
- **BMD Threats**
- **SUW**
- **TASW**
- **EMI / EMC**



Above Water Sensor Overview

New Development

SPY-3
S-VSR



CJR S
CJR X

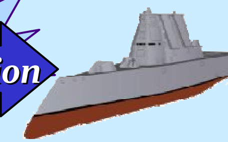
SPY-3 / VSR

DD(X)
CVN
LHA(R)

Cobra Judy Replacement Suite

CJR

Competition



CG(X)

LOW-COST RADAR R&D → LCS SENSOR SUITE → LCS (Radar Suite)

In-Service

SUSTAINING UPGRADES
LEGACY DIVESTMENTS

IN-SERVICE RADARS
(SPS-48 ROAR, SPQ-9B, etc) → Fleet Upgrades/ Backfits

LITTORAL WARFARE ENHANCEMENTS

SPY-1
In-service AEGIS → CG 47 Conversion
DDG 51 Midlife

Passive Sensors

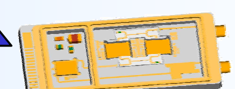
SEWIP → IN-SERVICE SLQ-32 → Fleet Upgrades & DD(X)

EO/IR SYSTEM

IROS3 & FOLLOW-ON → Fleet Upgrades, LCS, & DD(X)

Technology

SUPPORTING TECHNOLOGIES AND INTERNATIONAL COOPERATION



ONR, MDA, Int'l Cooperative Technology Efforts

Navy History in Shipboard Phased Arrays

- 60+ year track record of ship and phased array radar design, engineering, and construction
- Ongoing development of next-generation advanced shipboard phased array radars
- Clear understanding of shipboard power, cooling, and other auxiliary support systems

1983- present:

27 Aegis Cruisers; 44+ Destroyers

1960: USS Long Beach and USS Enterprise Search and Track Phased Arrays

1939: Battleship Gunfire Control Radar

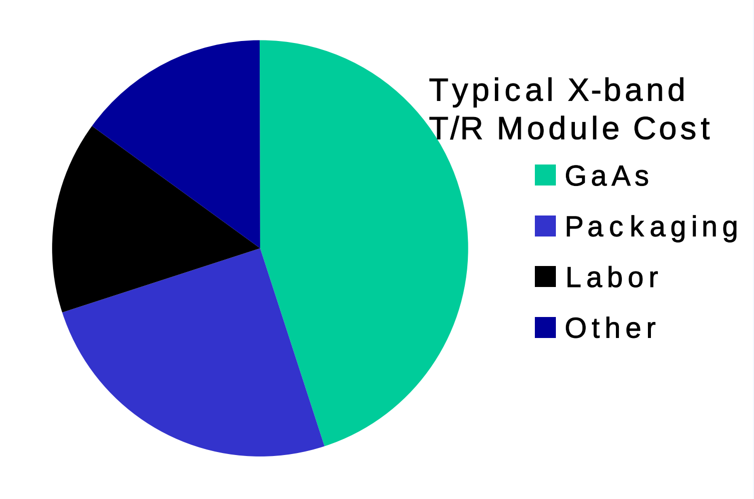
T/R Module Issues

- Technology supports most requirements
  - LV GaAs output power limitations
    - Can address by multiple HPAs per T/R module; Drives cost
  - HV GaAs satisfies most requirements
  - Wideband gap materials offer highest power potential
    - Thermal management and cost challenges
- LV GaAs in fielded systems
- HV GaAs in engineering development systems
- WBG devices in research and technology development
- High T/R module cost for long range RADAR applications
  - Large quantities of modules needed

Cost, not performance, is most challenging issue for future surface Navy applications

X-band T/R Module Cost Breakdown

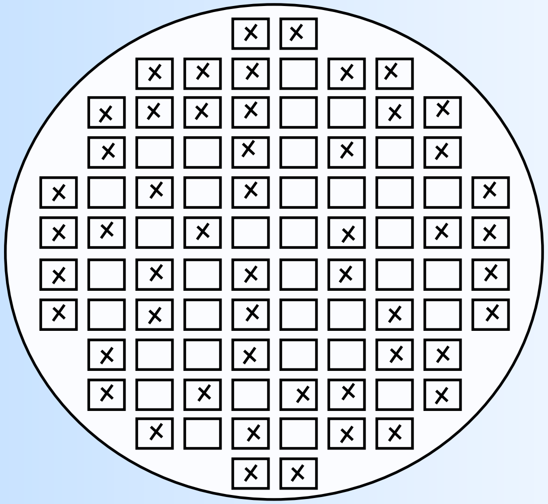
- Three major X-band T/R module cost elements
  - GaAs MMICs, packaging, and assembly
- Reduction in all areas for significant price cut
  - GaAs cost significantly varies among suppliers



MMICs are highest cost item and have greatest variation

MMIC Cost

- MMIC \$ = (Processed wafer \$) / (# of "good" MMICs/wafer)
  - Processed wafer cost drivers are labor and capital
  - # of good MMICs determined by wafer diameter, MMIC size, and yield



Top view of wafer showing MMICs and defective parts

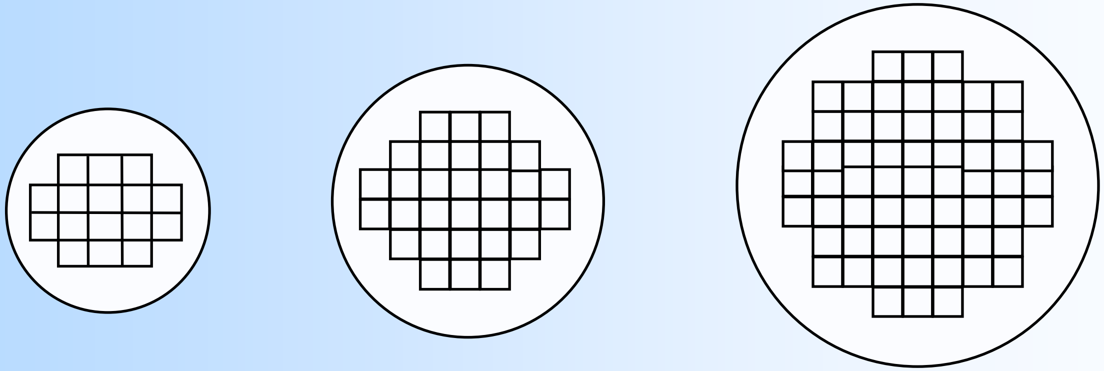
Wafer Processing Cost

- Capital and overhead costs vary widely among foundries
  - Foundry utilization = (Good wafers)/(Capacity)
  - Low foundry utilization increases cost by > 300%
- Volume often insufficient for low capital/overhead cost
  - GaAs foundry capacity = 10,000 - 50,000 4” wafers/yr
  - 100,000 10 W modules use ≈ 2,000 4” or 1,000 6” wafers
- High volume products using similar processes, not identical parts, necessary for low cost

Significant wafer volume necessary for low MMIC cost; MMIC volume driven by wireless applications

Wafer Diameter

- Larger diameter has more parts for similar wafer cost
- GaAs currently on 3” or 4”, some transition to 6”
- 6” processing requires large capital investment
  - High volume necessary to offset capital cost
  - Technical issues; Breakage and uniformity



3”

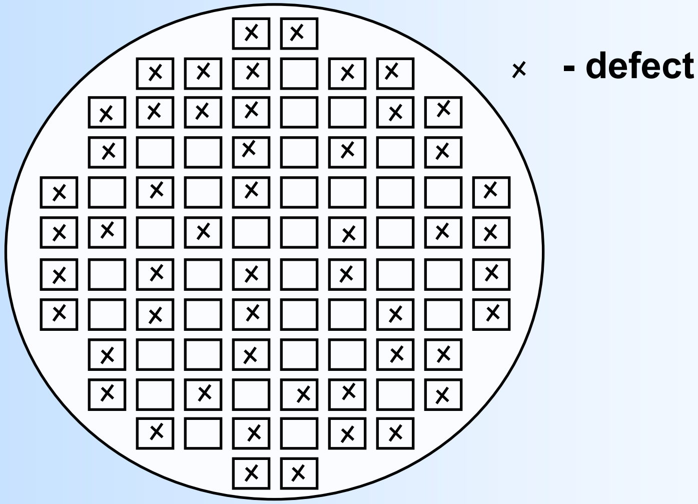
4”
≈ 2x’s # of 3” MMICs

6”
≈ 2x’s # of 4” MMICs

Transition to 6” wafers driven by volume, not cost

Size/Complexity and Defects

Lower Power MMIC



40% MMIC Yield
(25-50% typical for ≈ 5 Watts)

- Smaller die less expensive/higher yield; Complexity drives yield
- High process yield enables higher power and higher integration
  - Current commercial devices will not drive improvements

High complexity control and PA MMICs stress yields and drive cost

T/R Module Assembly

- Wire bond and pick and place assembly is highly automated
  - High assembly yields (> 90%) can be achieved
  - Total direct labor time can be < 1 hour per module
  - Bond wire reliability not an issue; Missed, rather than weak, wire bonds made by robotics
- Flip-chip and ball-grid arrays can reduce assembly time
  - Introduces CTE-based reliability and design issues; Issue is more severe as integration/size increases
  - Batch (parallel) rather than serial assembly process
  - Eliminates cost of backside processing, but adds additional cost of wafer bumping

Bondwire-based assembly can be reliable and low cost

T/R Module Packaging

- Packaging satisfies performance
  - Low loss only critical after PA and before LNA
  - Thermal management can be an issue for high power MMIC applications
- Cost reduction is remaining issue
  - Thick-film, rather than thin-film, on low cost substrate
- Different requirements within a module; No traditional T/Rs
  - PA and LNA needs high performance, low I/O; Single layer, gold ink, thick-film substrate
  - Control MMICs needs low performance, high I/O; Multiple layer, thick-film conductor

Movement to lower cost, lower performance substrates and modified packaging architectures

Cost Determines Technology Choice

X-Band
2P W Module
SiC or GaN

16,750 Elements
7.5 ft Diameter

Wide Bandgap Technology

vs.

X-Band
P W Module
GaAs

33,000 Elements
11 ft Diameter

Current Technology

Equivalent Performance Tracking Radars

- Higher power module lowers number of T/R modules and area
  - Requires more MMIC power, prime power, and cooling
- For many high power applications cost will drive technology choice

Future Trends for Phased Arrays

- Use of foundries with high loading
- Move to larger wafers driven by other applications
- Development to improve yields
  - Power amplifier and control MMIC complexity lowers yield compared to simpler components
  - Significant cost reduction potential (> 2X)
  - Enables lower cost packaging/assembly by enabling higher level of integration
- Semiconductor cost reduction through improved processes
  - Also enables higher integration to reduce packaging and assembly costs
- Utilize lower cost, lower performance packaging materials
- Cost and power are stressing future requirements
- Wide bandgap to address output power/cost issues
  - Metrics other than power density necessary to evaluate progress
  - Material quality key to scaling proof-of-concept devices to higher powers with same power density